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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,645	09/18/2003	Thomas S. Wong	MIC-M082	6083

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EXAMINER	
TAN, VIBOL	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 01/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/665,645	WONG ET AL.	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-10 and 12-15* is/are rejected.

7)☒ Claim(s) *5,6 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/18/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Figure 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. Please use correct symbol to identify Schottky diodes in drawing.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 4, 7-10, 12, 14 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Morris et al. (U. S. PAT. 4,898,838).

In claim 1, Morris et al. teaches all claimed features in Figs. 9-10, a monolithic integrated circuit comprising a plurality of logic gates, a single logic gate comprising: a P-type well (34) formed in an N-type region (24), the P-type well forming a base (34) of an NPN bipolar transistor (63); an N+ region (50) formed in the P-type well forming an emitter (50) of the bipolar transistor; the N-type region (24) forming a collector (12) of

the transistor in common with the cathodes of two or more Schottky diodes (74s); and nodes (node at end of 36, 126,128) of the logic gate being adapted for coupling to nodes of other similar logic gates , the nodes of the logic gate comprising an input node (the node at end of 36) coupled to the base and comprising output nodes (126, 128) coupled to respective anodes of the two or more Schottky diodes (74s).

In claim 2, Morris et al. further teaches the circuit of Claim 1 wherein the two or more Schottky diodes comprise one or more output Schottky diodes (74s) and at least one clamping Schottky diode (59), the at least one clamping Schottky diode being coupled between the collector (12) and base (34) of the transistor.

In claim 4, Morris et al. further teaches the circuit of Claim 2 wherein an anode of the at least one clamping Schottky diode comprises titanium or titanium silicide (col. 1, line 60).

In claim 7, Morris et al. further teaches the circuit of Claim 1 wherein the N-type region is a portion of an N-type epitaxial layer (24), the portion being electrically isolated from other portions of the epitaxial layer.

In claim 8, Morris et al. further teaches the circuit of Claim 1 wherein the N-type region (24) is an N-type well formed within a P-type material (P-substrate).

In claim 9, Morris et al. further teaches the circuit of Claim 1 further comprising an anode metal (terminal) of each of the two or more Schottky diodes in contact with the N-type region (24, 12).

In claim 10, Morris et al. further teaches the circuit of Claim 9 wherein the anode metal of at least one Schottky diode comprises aluminum (col. 2, line 1) or aluminum silicide.

In claim 12, Morris et al. further teaches the circuit of Claim 9 wherein the anode metal of at least one Schottky diode comprises titanium (col. 1, line 60) or titanium silicide.

In claim 14, Morris et al. further teaches the circuit of Claim 1 wherein anodes of the two or more Schottky diodes are coupled to respective bases of additional NPN bipolar transistors (each 126 and 128 coupled to base 34 of other 63, respectively; not shown).

In claim 15, Morris et al. further teaches the circuit of Claim 1 further comprising multiple logic gates being interconnected such that anodes of the two or more Schottky diodes are coupled to respective bases of bipolar transistors via one or more metal layers (col. 5, lines 63-67).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morris et al.

In claim 3, Morris et al. teaches all claimed features of claim 2; with the exception of showing a resistor in series with the at least one clamping Schottky diode. However, it is obvious to one ordinary skill in the art to place a resistor in series with the claiming diode, as claimed, because a resistor in series act as a voltage divides.

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to place a resistor in series with the Schottky diode 59 of Morris et al. to drop some voltage.

7. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morris et al. in view of H.H. Berger et al.

In claim 13, Morris et al. teaches all claimed features the circuit of claim 1; with the exception of teaching wherein the logic gate forms a portion of NAND function. However, Berger et al. teaches in page 90, Fig. 4, the logic gate forms a portion of NAND function.

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to form a portion of NAND function using the circuit of Morris et al. to improve the speed limit and to reduce the number of active silicon regions.

8. Claims 5, 6, and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vibol Tan

Primary Examiner, AU 2819

VIBOL TAN
PRIMARY EXAMINER